

FIG. 1

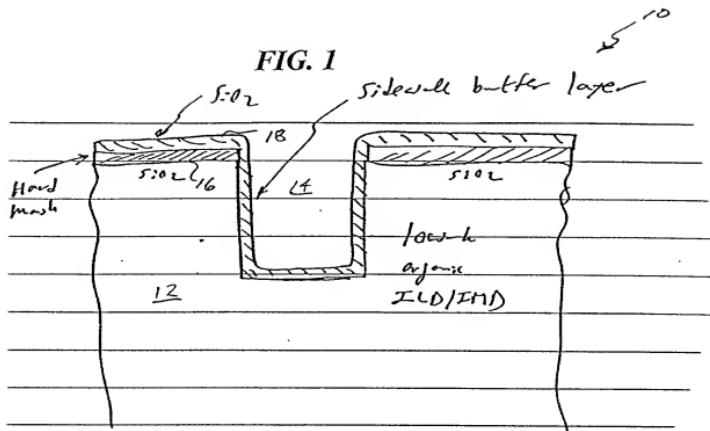
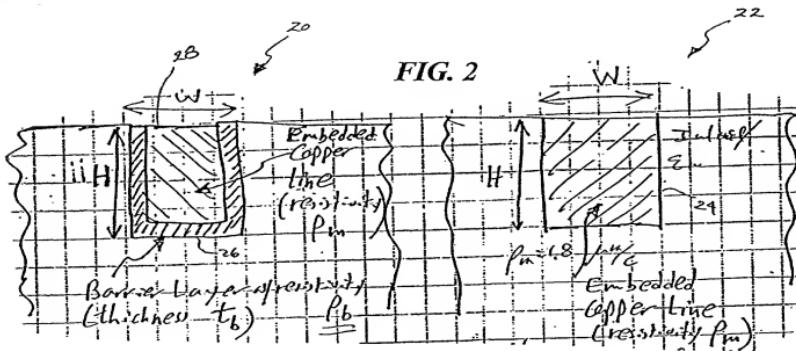


FIG. 2



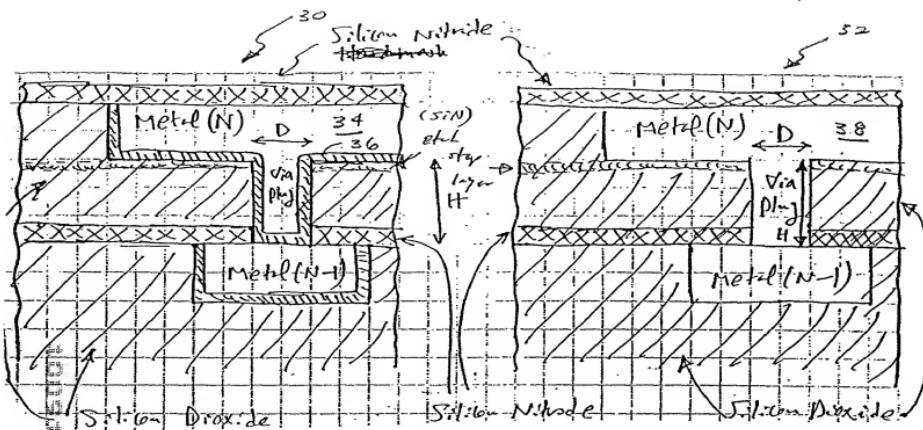


FIG. 3

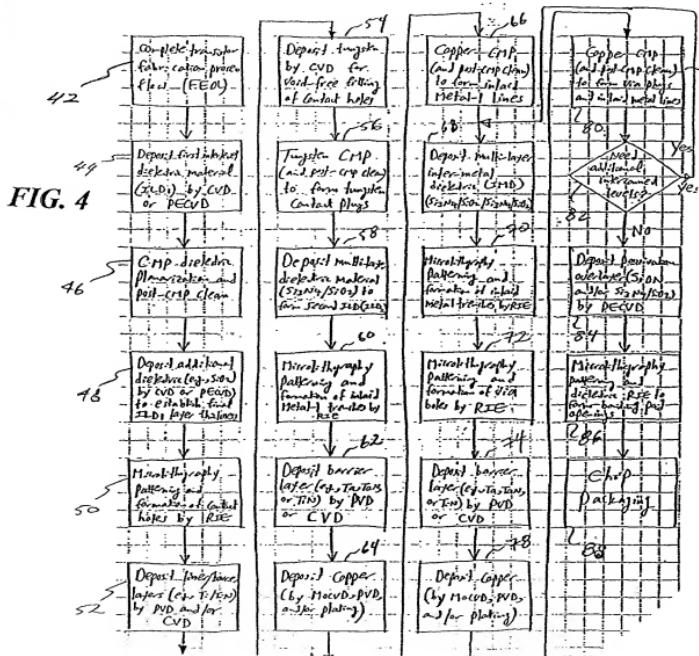


FIG. 5

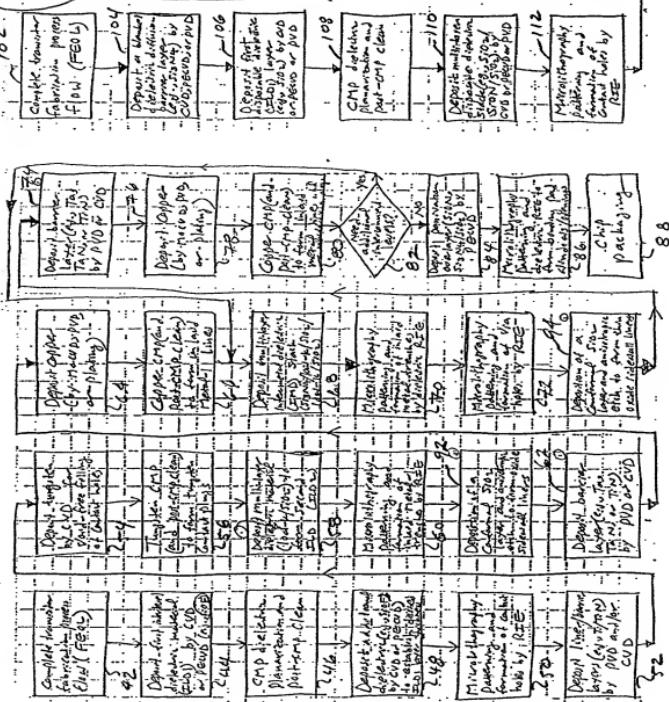
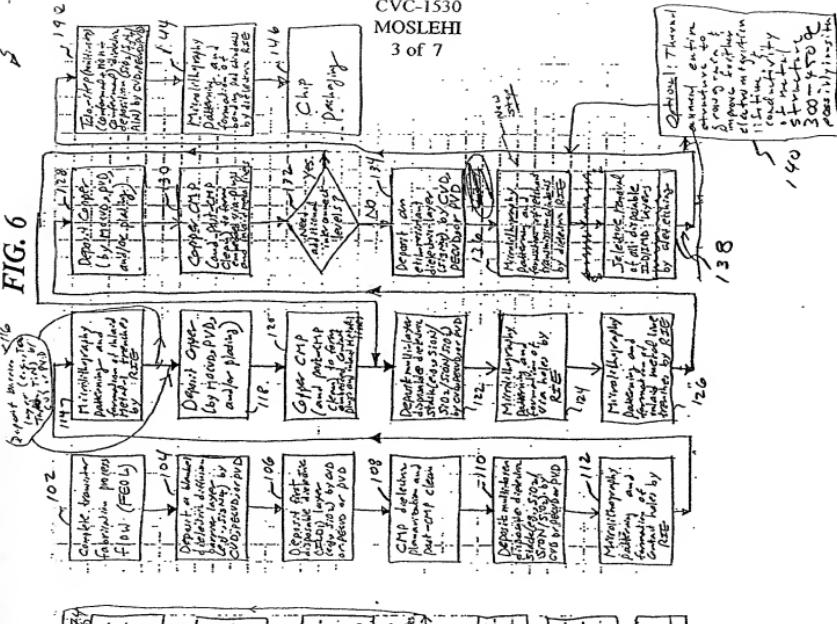


FIG. 6



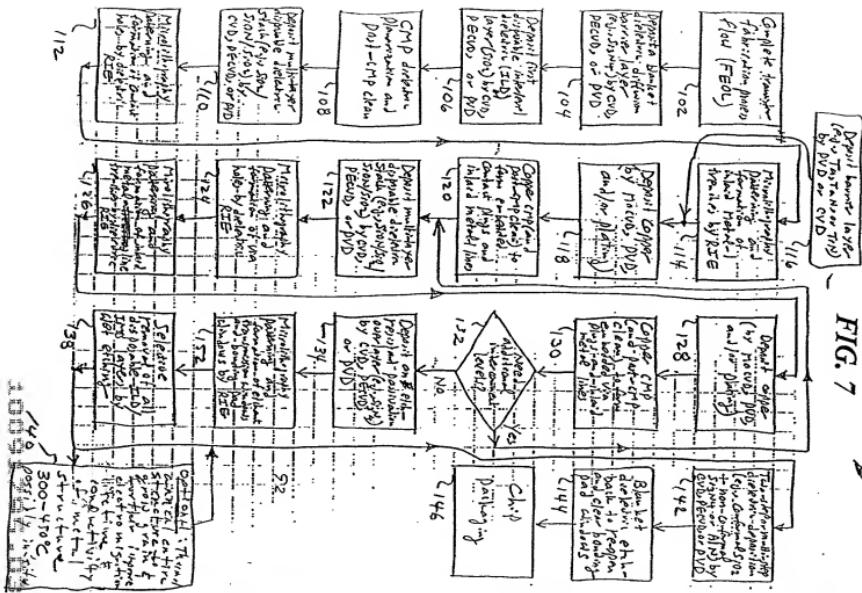


FIG. 8 Top Layer of Etch-Resistant Dielectric (Silicon Nitride or Aluminum Nitride)

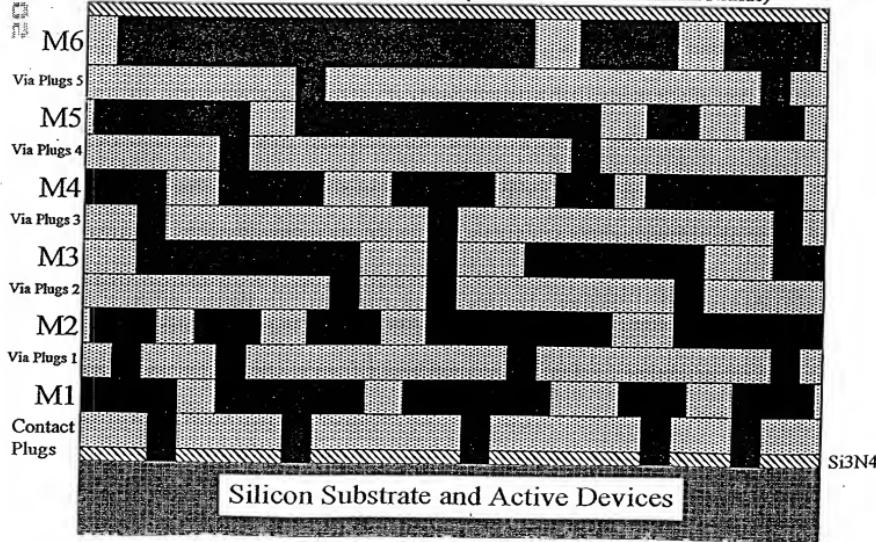


FIG. 10

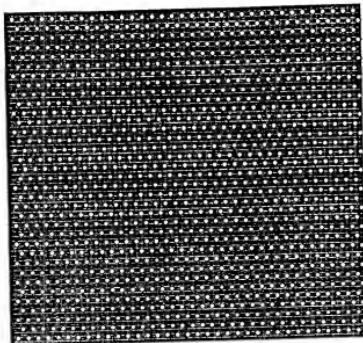
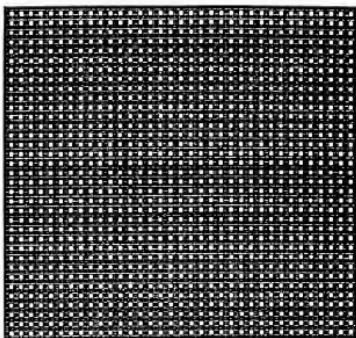


FIG. 9



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FIG. 12

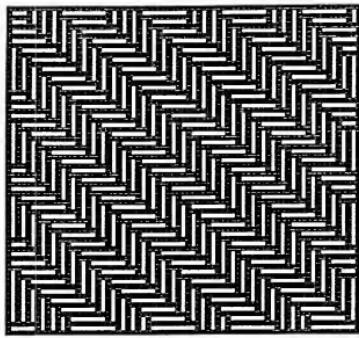


FIG. 11

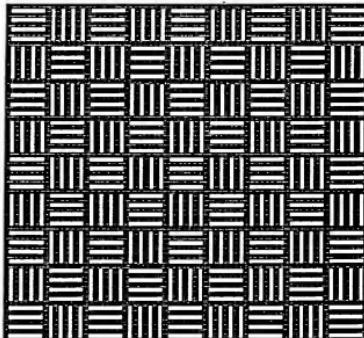


FIG. 13 Top Layer of Etch-Resistant Dielectric (Silicon Nitride or Aluminum Nitride)

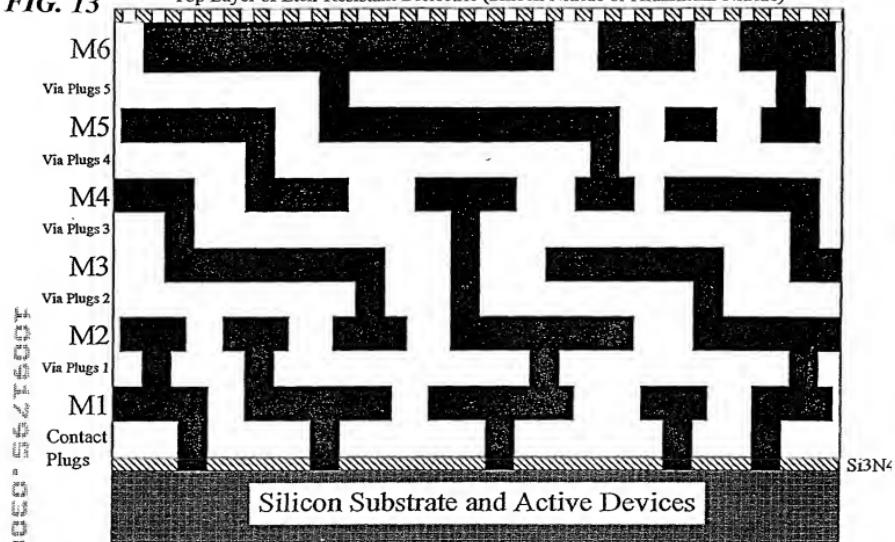
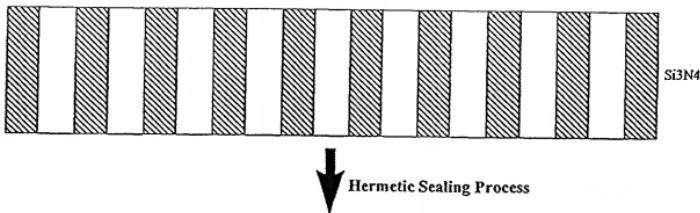


FIG. 14

Top dielectric layer (e.g., Si₃N₄) with etchant transmission windows (e.g., minimum geometry holes)



After conformal deposition of first dielectric (e.g., CVD SiO₂ or Si₃N₄ or AlN) followed by non-conformal deposition of second sealing dielectric (e.g., PVD of AlN or DLC or Si₃N₄)

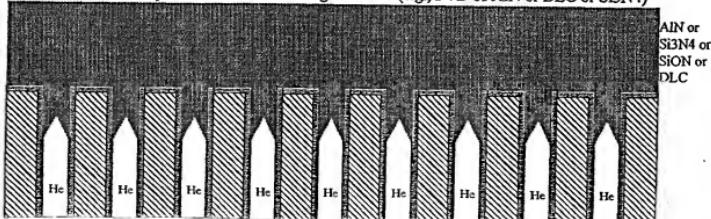


FIG. 15

High-Thermal-Conductivity Hermetic
Sealing Insulator (SiO₂/AlN, SiO₂/DLC, etc.)

